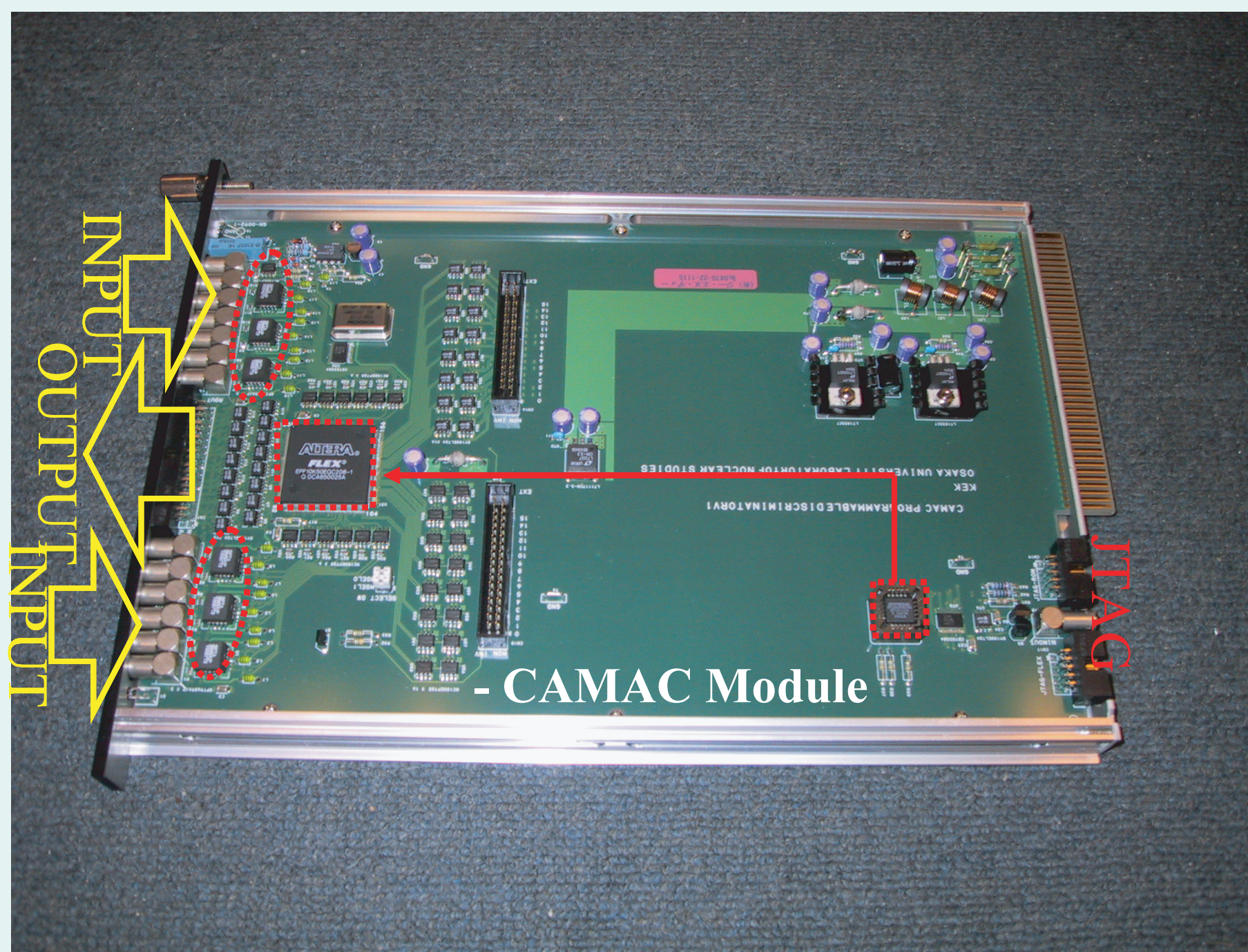# - *Digital Mean-timer module*

In E787, analog sum signals of the single end of the RS and BV counters were used for the photon veto signal, and the veto time width was large to account for the timing variations due to the z-position of the photons. By using a Mean-timer module, the veto time width can be narrowed and accidental veto rate is therefore reduced.


- CAMAC Module

The signals of both ends of the RS, BV and BVL counters are mean-timed in the Mean-timer. The mean-timed signals are used as L0 photon veto signal.

Large-Scale PLD	EPF10K50E-1
Board Size	CAMAC
Input	12 analog at front
Output	16 ECL at front

FIG. 7. A picture of the Mean-timer module.
A large-scale PLD is located at middle-left of the module.
Due to space limitation in the electronics hut, the module combined the functions of a discriminator and PLD.

The performance of the Mean-timer was tested at a test bench. Two random signals from gate generators are input to the Mean-timer module. The two input signals and the mean-timed signal are fed into a CAMAC TDC with 25psec resolution. The left plot is the time distribution of the two inputs signals. Since the 12 delay-cells in a delay-line are used for this test, the range is 12nsec. The right plot is the time distribution of the difference of the online and offline mean-timed signals. The sigma is 0.26nsec.
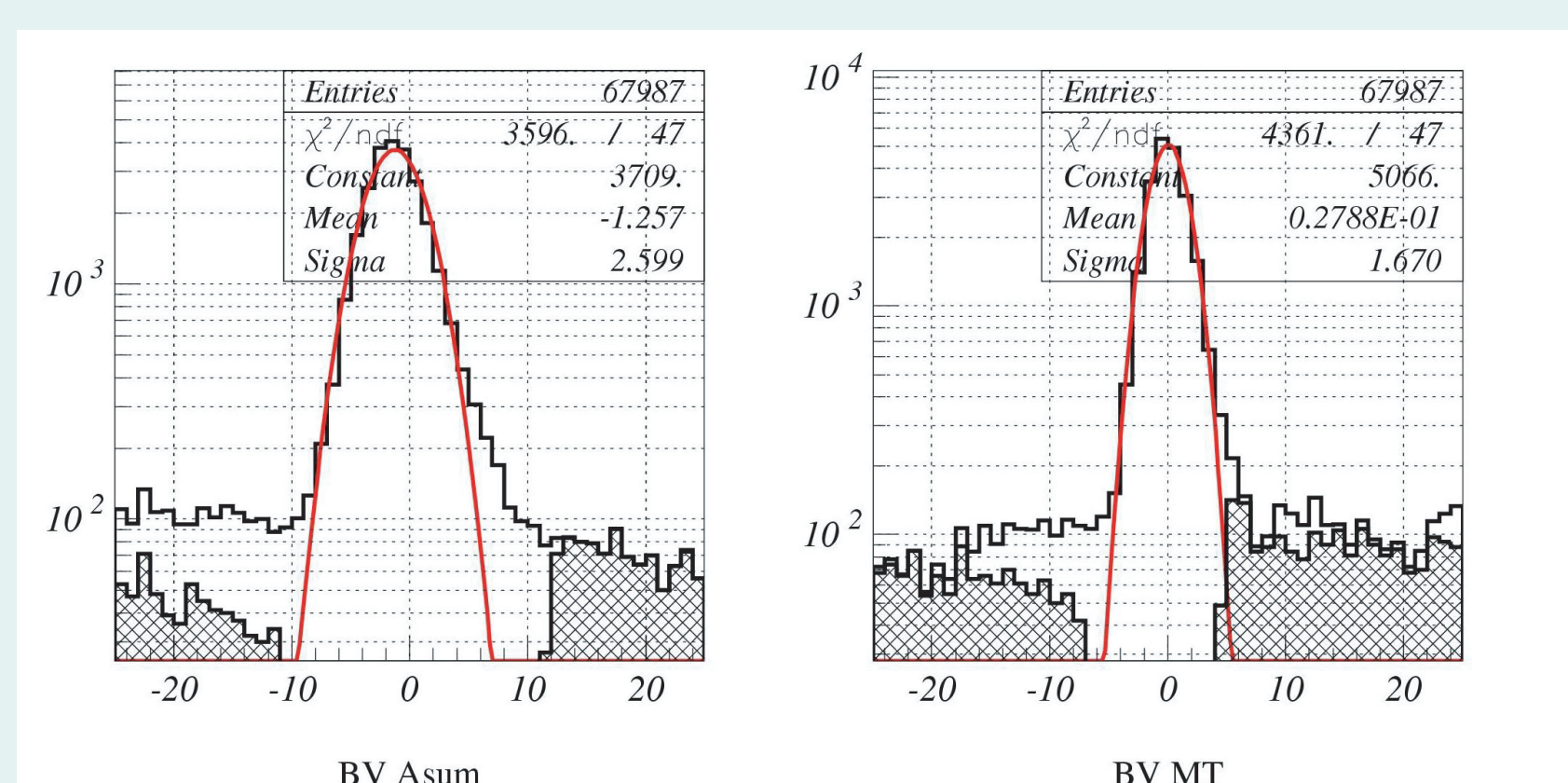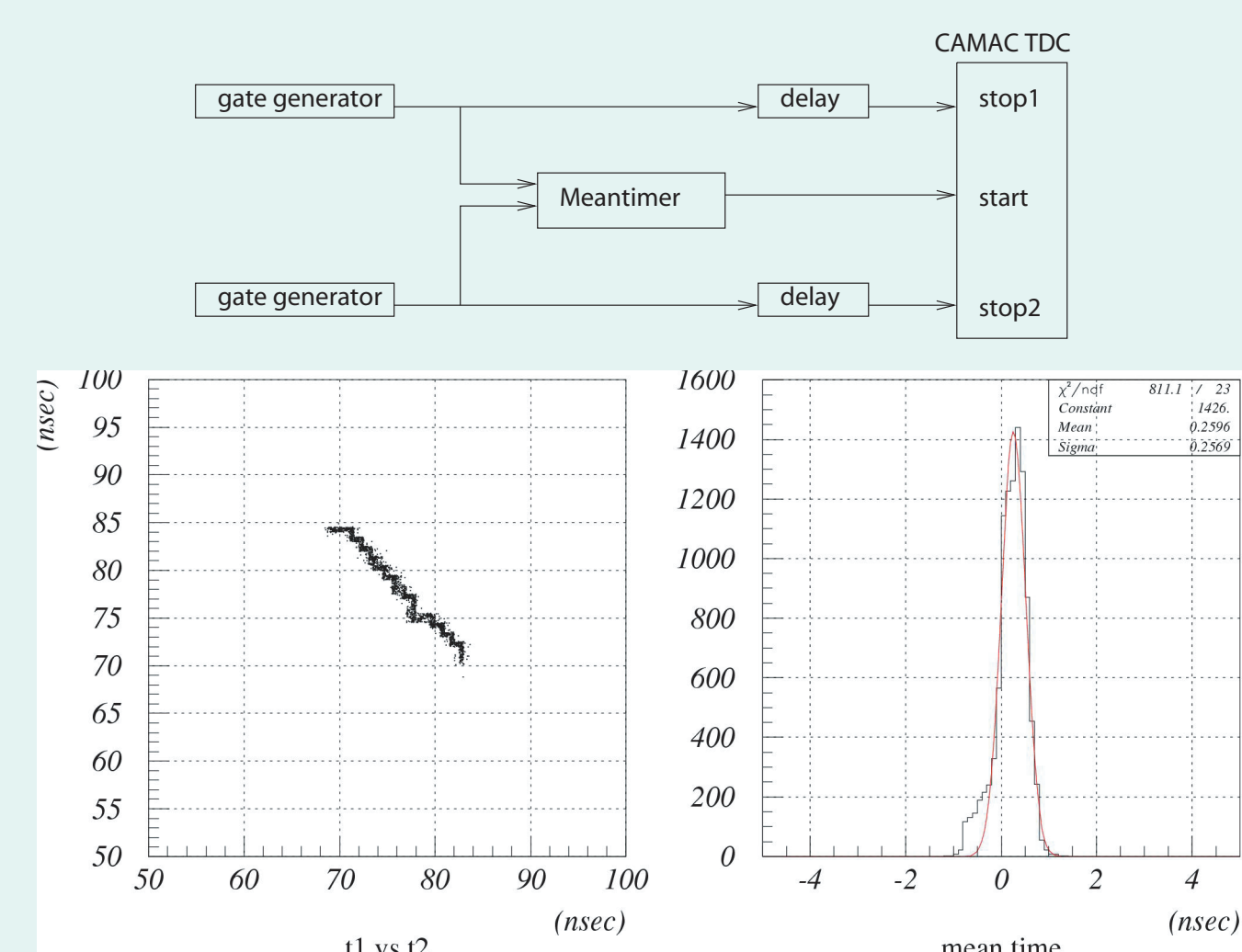
The digital Mean - timers were installed to the E949 trigger system and the performance was checked. Left figure shows the time distribution of analog sum signal and right figure shows the distribution of digital Mean - timer signal. Open histogram shows $K^+ \rightarrow \pi^+ \pi^0$ distribution of hit times in the photon veto bit is not set. Shaded histogram shows the time distribution for events with the bit set. In all cases the time distributions of the photon veto signals is shown relative to the time of the π^+ track. The hits at around $t = 0$ due to electromagnetic shower in the detector were removed efficiently with half the acceptance loss of the previous system.

- *Summary*

We have developed the L0 trigger board and digital Mean-timer module for the BNL-E949 experiment. The L0 trigger board allowed us rapid and simple programming of the triggers. In addition to the flexibility, the online dead time was reduced by on-chip prescaler. A powerful diagnostic capability provided quick and easy debugging of the new trigger logic. The digital Mean-timer modules were installed to reduce online dead time. Using the modules, a factor of two narrower veto width has been realized.